TESTING APPARATUS AND METHOD FOR THIN FILM TRANSISTOR DISPLAY ARRAY

ABSTRACT

~~The present invention discloses a~~A testing circuit and method for thin film transistor display array, for testing the yield of a thin film transistor array is provided. The testing circuit ~~comprising: An~~includes an array tester, a test panel (DUT)[[,]]and a sense amplifier array. The sense amplifier is composed [[by]]of a plurality of trans-impedance amplifier units and a plurality of parasitic capacitance discharge circuit units. Every sense amplifier includes[[:]] a trans-impedance amplifier, which is implemented by an operational amplifier, two switches and an operation capacitance~~, the~~. The trans-impedance amplifier is used to form an integrated circuit[[,]] and the output is transmitted to a sampling/hold circuit via a switch[[; a]]. Also included is a parasitic capacitance discharge circuit that is used to form a discharge route for the charge of the parasitic capacitance.